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# Investigation on Thermal Cycling Life Prediction of PBGA Microprocessor Components with Wavy Patterned Interface Layer

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**Abstract.** In modern electronic packaging industries, plastic ball grid array (PBGA) has been widely used as the microprocessor components. Upon thermal cycling due to the generation of thermal stresses, the PBGA package may undergo fatigue failure in the solder balls and thus it became a matter of interest for researchers to model the PBGA package to calculate its thermal cycling life. This study aims in 3D finite element modeling of the slice model of a PBGA package to calculate the accumulated plastic dissipation energy per cycle in the solder joint, which is often considered as an indication of damage accumulation in the solder joint of the PBGA package. The thermal cycling simulation is performed between -40 to 125 °C and the associated life to failure is predicted using obtained finite element results and life prediction theory. As researchers have already showed, the failure of the solder joint usually starts at the corner of the solder-copper interface layer and then it propagates along the interface or through the body of the solder depending on the mechanical properties and shape of the solder ball. Traditionally, a flat interface layer is always maintained in the manufacturing of the PBGA packages. For the first time, this research focuses on the effects of the interface geometry on the damage accumulation in the critical solder joint hence the life for crack initiation as well as crack propagation of the package. Instead of a flat circular solder-copper interface layer, a wavy patterned interface layer is considered in the simulation. Finite element analysis results show that thermal life and crack propagation in the solder ball greatly depends on the geometry of the solder joints. The volume averaged plastic energy dissipation accumulated per cycle is reduced when a wavy patterned interface layer is considered which may be due to the fact that more surfaces come in contact with each other reducing stress and therefore the no. of cycles before failure increased in case of wavy patterned interface layer.

## INTRODUCTION

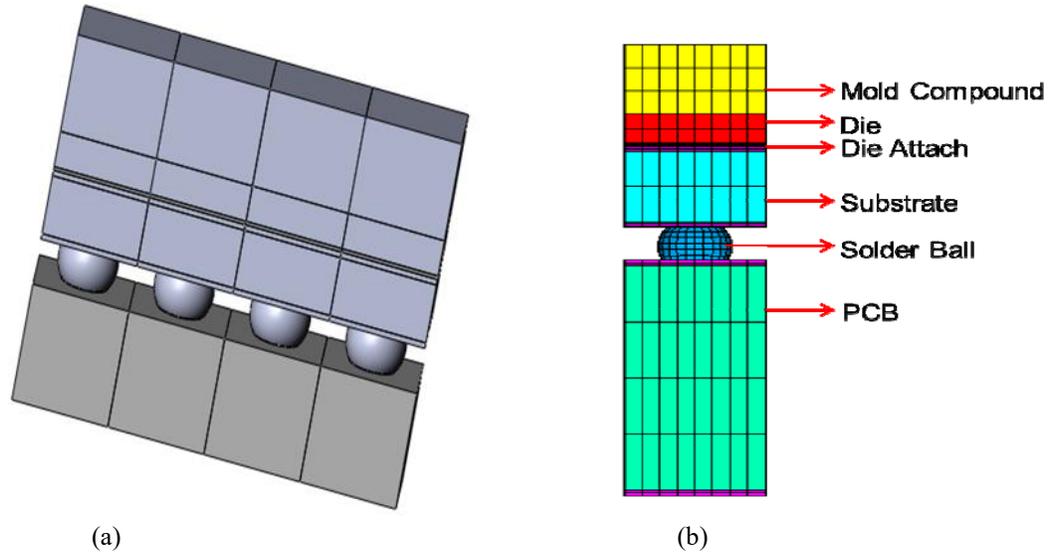
Following the advancement of semiconductor and packaging technology, plastic ball grid array (PBGA) has become more popular in the electronics industry due to its cost effectiveness and the ease of implementation. In recent times, modern microprocessors deal with different harsh environment which often leads to fatigue failure in the solder ball joint as a result of temperature fluctuation. To predict the thermal life of PBGA package, finite element simulations of Accelerated Life Testing (ALT) for the PBGA assemblies are normally performed using thermal cycling. In ALT method, the temperature fluctuation is provoked than the normal temperature exposure this package should handle which allows to uncover faults and potential modes of failure in a short period of time [1]. In 2014, Ping, et al. [2] investigated the thermal stress and strain of Plastic Ball Grid Array (PBGA) for reliability evaluation and failure analysis. Thermal cycling temperature of (0°C–100°C) in a one-eighth model is developed to calculate the thermal stress and strain on PBGA package and the results show that the maximum equivalent stress and equivalent plastic strain occur in the second outer solder joint and close to the position of chip. In order to increase the reliability and manufacturing ability, Sung, et al. [3] suggested a design guideline for PBGA package. The chip dimension and the thickness of the substrate layer plays a crucial role on the solder joint reliability of

plastic ball grid array packages [4]. The failure of the solder joint usually starts at the corner of the solder-copper interface layer and then it propagates along the interface or through the body of the solder depending on the mechanical properties and shape of the solder ball. The substrate material is placed just above the solder ball layer and these solder balls are also attached to the printed circuit board (PCB) at the bottom side. Traditionally, a flat interface layer is always maintained in the manufacturing of the PBGA packages between the solder ball and copper layer.

This study has been performed to investigate how the predicted life of a PBGA microprocessor changes when the solder-copper interface geometry is changed and the effects of interface geometry instead of flat interface layer would have on the thermal life and crack propagation on PBGA packages. This research focuses on the effects of the interface geometry on the damage accumulation in the critical solder joint hence the life for crack initiation as well as crack propagation of the package. Instead of a flat circular solder-copper interface layer, a wavy patterned interface layer is considered in the simulation. The simulation results showed the possibility of less amount of volume averaged energy dissipation accumulated per cycle in wavy patterned interface layer which thus indicates great potential in considering other than flat circular pattern in solder-copper interface layer.

### FINITE ELEMENT MODELING OF THE PBGA PACKAGE

To calculate the accumulated strain energy dissipation per cycle in the solder joints by accelerated life testing (ALT) method for PBGA packages, thermal cycling simulation was performed between -40 to 125°C and the associated life to failure was predicted using finite element results and life prediction theory. The half slice model of the PBGA package was developed and solved using ANSYS finite element software. Three dimensional nonlinear finite element modeling of microprocessor packaging was used to estimate accumulated strain energy dissipation per cycle in the solder joints as a result of thermal cycling between -40 to 125°C. Figure 1 shows the half slice model geometry as well as the unstructured meshed model along the diagonal elements of the PBGA package that was developed and solved using ANSYS finite element software.



**FIGURE 1.** (a) Geometry of the diagonal element of half slice model (b) Unstructured meshed elements shown in PBGA microprocessor. Different colors define distinguishable materials in the microprocessor assembly.

The model has been constrained along the axes of symmetry, thus the displacement component of all the nodes perpendicular to the symmetry plane was assumed to be zero in that direction. In addition to that all the Degrees of freedom in the central nodes at that plane are assumed to be zero to resist rigid body motion in PBGA microprocessor. The solder balls were modeled using ANSYS with Solid185 structural elements with 8 nodes similar to that done by Motalab, et al., 2015[5]. This element is well recognized to solve both isochoric (volume

preserving) large strain plasticity problems. Those elements appears to have plasticity, creep and large strain problem solving capabilities. Iterative solution procedures have been used to model nonlinearity and kinematic properties. The entire assembly was subjected to pulsating temperature distribution of -40 to 125°C to replicate thermal cycling in life testing experiments. Ramp rate for this thermal cycle is selected to be 16.5 °C/min, and the dwelling time for peak temperatures were taken to be 20 minutes. The solidification temperature of the lead free solder joints is  $T = 220$  °C and it was assumed to be the stress free-temperature. The applied thermal loading was taken to be the same as done by Motalab, et al., 2015 [5] and the applied thermal loading is shown in Fig. 2 from Motalab, et al., 2015. The solder balls have been modeled as visco-plastic material with the Anand model (Motalab, et al., 2013) [6]. The properties of other materials have been used as listed in table 1(Motalab, et al., 2013).

In our study we have focused on the effects of the interface geometry on the damage accumulation in the critical solder joint hence the life for crack initiation as well as crack propagation of the package. Figure-3 shows the solder-copper interface of that were considered, first a regular type flat interface followed by two wavy patterned interface layer to predict life of a PBGA microprocessor.

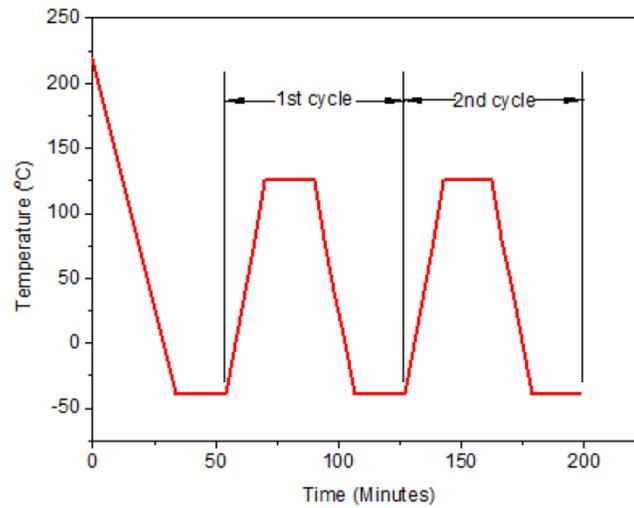
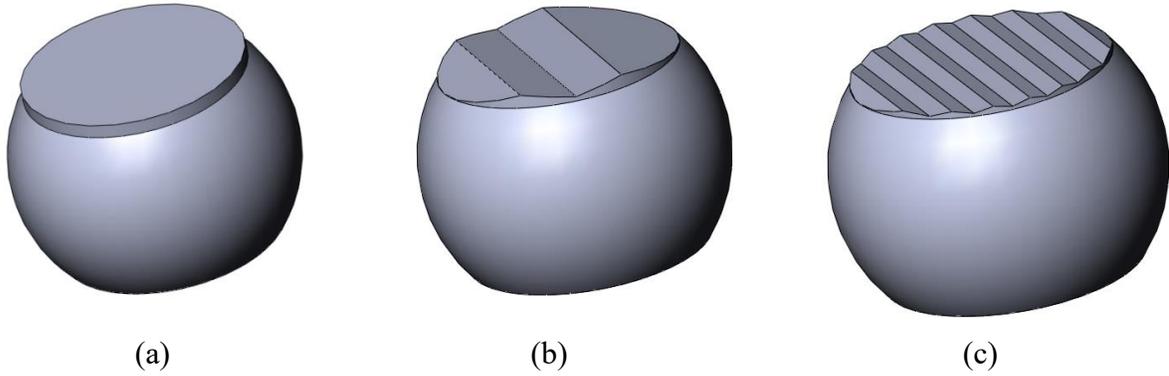


FIGURE 2. Applied thermal loading (b) Room temperature material properties used in the PBGA model

TABLE 1. Room temperature material properties used in the PBGA model

Material	Elastic Modulus (Gpa)	Poisson's Ratio	CTE(ppm/C)
PCB	$E_x = 16.90$	$PR_{xy} = 0.39$	$CTE_x = 14.5$
	$E_y = 7.44$	$PR_{yz} = 0.39$	$CTE_y = 67.2$
	$E_z = 16.90$	$PR_{xz} = 0.11$	$CTE_z = 14.5$
Solder Mask	3.1	0.3	16.3
Copper Pad	128	0.34	17
Die Attachment Adhesive	1.5	0.35	$65 (T < T_g)$
			$200 (T > T_g)$
			$T_g = 60$ °C
Die	169	0.28	2.54



**FIGURE 3.** Different solder ball configurations (a) For flat interface layer (b) Flat interface surface was changed to wavy interface (c) waviness increased

## RESULTS AND DISCUSSION

Three dimensional nonlinear finite element modeling of microprocessor packaging was used to estimate accumulated strain energy dissipation per cycle in the solder joints as a result of thermal cycling between -40 to 125°C. The effects of the interface geometry on the damage accumulation in the critical solder joint hence the life for crack initiation as well as crack propagation of the package was observed. Instead of a flat circular solder-copper interface layer, a wavy patterned interface layer was considered in the simulation. At first a regular type flat interface was simulated which was followed by two wavy patterned interface layer to predict life of a PBGA microprocessor. In this study of microprocessor packaging, the critical solder ball in the diagonal PBGA assembly was found to be located near the package corner. The volume averaged plastic energy dissipation  $\Delta W$  accumulated per cycle is considered to be the parameter for damage accumulation and failure criterion for solder joints. Figure 4 shows  $\Delta W$  distribution for flat solder ball arrangement as well as for wavy interfacial solder ball arrangement whereas Fig. 5 shows variation of  $\Delta W$  distribution between critical solder balls of both arrangements. It can be noted that  $\Delta W$  value has decreased for wavy interface just into the half value compared with the flat one. This means that the strategy of choosing wavy interface rather than the flat one has a favorable effect on the increased life of the PBGA solder ball as well as the reliability of the microprocessor life. The estimated reason for this enhancement in microprocessor life cycle could be the better coupling between the SAC solder ball and Copper pad which offers more amount of surface area in contact which rather reduces the stress and overcomes the effect of increased stress concentration due to non-uniform contact. It can be stated too that maximum stress is generated in the corner of the interface in curved interface solder balls rather than distributed all over the interface due to rough contact in case of flat solder balls. It can be shown that in Fig. 4 the corner solder ball has the maximum  $\Delta W$  dissipation compared to others. Using Energy dissipation based models for life prediction in solder joints subjected to cyclic loading Darveaux, 2000 [7],

$$N_i = K_1 (\Delta W)^{K_2} \quad (1)$$

$$\frac{da}{dN} = K_3 (\Delta W)^{K_4} \quad (2)$$

Where these equations represent the model for crack initiation and the model for Crack Growth simultaneously. From [7],  $N_i$  is the number cycles to crack initiation,  $da/dN$  is the crack growth rate occurring after crack initiation (which was assumed constant here),  $\Delta W$  is the energy dissipation per cycle in the solder sample and  $K_1$ ,  $K_2$ ,  $K_3$  and  $K_4$  are fitting constants from [6]. The number of cycles to failure can be estimated after we know the crack location and the path in the solder joint from [7] by,

$$N_f = N_o + \frac{a_c}{\left| \frac{da}{dN} \right|} \quad (3)$$

Where  $N_F$  is the number of cycles to failure and  $a_c$  is the length of the fully developed crack at failure. Figure 6(a) shows the variation of  $\Delta W$  with percentage of increase in area in the interface. Assuming non-aged configuration, Cycles of failure is predicted in Figure 6(b).

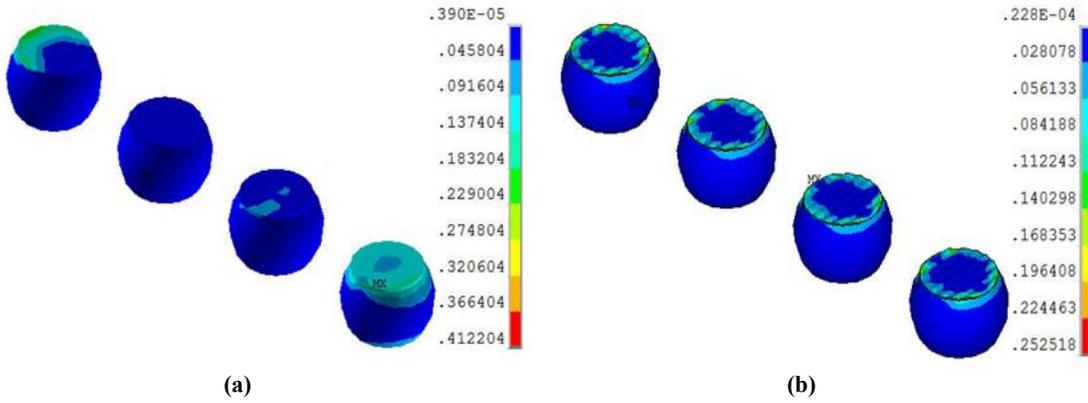


FIGURE 4.  $\Delta W$  distribution (a) For flat solder ball arrangement (b) For wavy interfacial solder ball arrangement

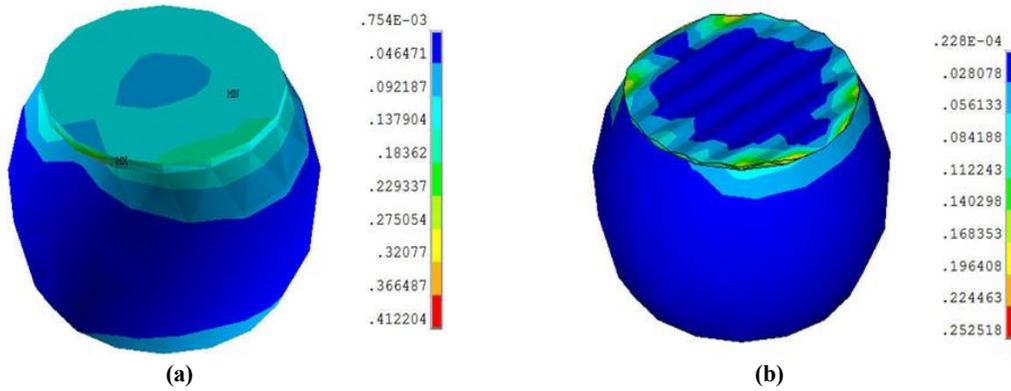


FIGURE 5.  $\Delta W$  distribution for critical solder ball (a) For flat solder ball arrangement (b) For wavy interfacial solder ball arrangement

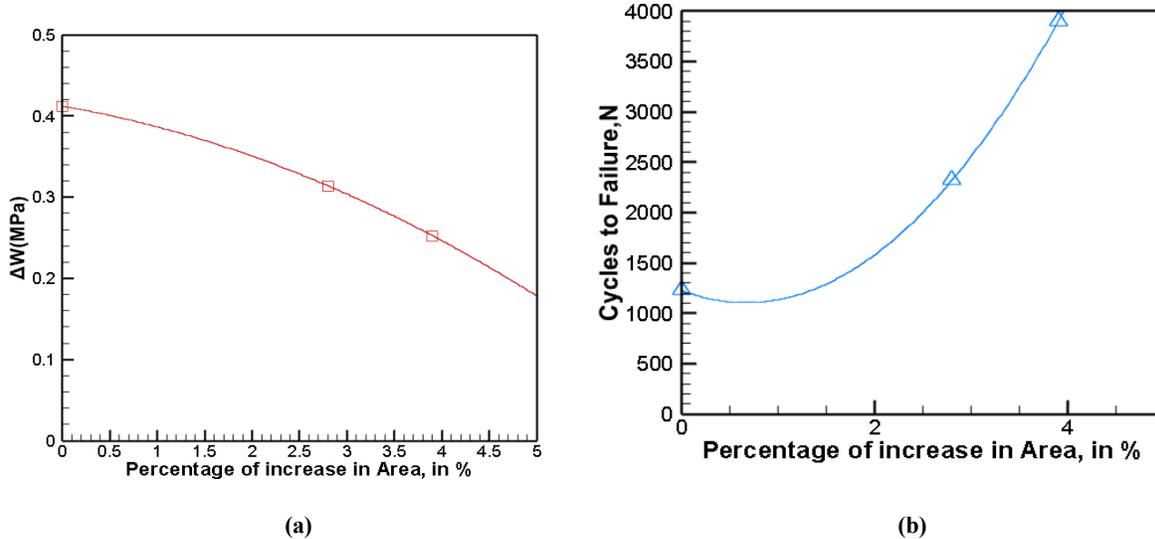


FIGURE 6. Shows the variation of (a)  $\Delta W$  with the number of wedges (b) Cycles to failure with number of wedges.

## CONCLUSIONS

The effects of wavy patterned solder-copper interface on the thermal cycling life (life of solder balls) of the PBGA (plastic ball grid array) microprocessor have been investigated in this research. The half slice model of the PBGA package that was developed and solved using ANSYS finite element software, used to estimate accumulated strain energy dissipation per cycle in the solder joints as a result of thermal cycling between -40 to 125°C. Instead of a flat circular solder-copper interface layer, a wavy patterned interface layer was considered in the simulation and the volume averaged plastic energy dissipation  $\Delta W$  accumulated per cycle has been calculated. The simulation results showed that, the  $\Delta W$  has decreased in case of wavy pattern interface than for flat circular interface layer. The increased in waviness also played a crucial part in the value of  $\Delta W$ . By minimizing the value of  $\Delta W$ , we observe a significant increase in cycles to failure of solder balls. However, this particular research need further development in order to find a suitable geometry for solder-copper interface layer which thus maximize the number of cycles to failure of the solder balls.

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